**Assignment 9**

**Assignment** All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

1. Write the Verilog code and testbench for serial in serial out shift register.

<https://www.edaplayground.com/x/asCR>

1. Write the Verilog code and testbench for serial in parallel out shift register.

<https://www.edaplayground.com/x/7b2s>

**Self-Practice and self-evaluation (Very Important)**

4-bit shift register: Below is the code for shift register using blocking statements. Write the testbench for the same and identify the issues when using blocking statements.

*module shift\_reg (output reg A, input E, clk, rst);*

*reg B, C, D;*

*always @ (posedge clk, posedge rst) begin*

*if (rst == 1’b1) begin*

*A=0;*

*B = 0;*

*C = 0;*

*D = 0;*

*end*

*else begin*

*A = B;*

*B = C;*

*C = D;*

*D = E;*

*end*

*end*

*endmodule*